T01. Practical ESD Protection Co-design Techniques for ICs, Modules, and Systems

Prof. Albert Wang (University of California, USA)

Electrostatic discharge (ESD) failure is one of the biggest IC reliability problems. As IC technologies advance into the very-deep-sub-micron and nano nodes, on-chip ESD protection design quickly emerges as a grand IC design challenge to all IC designers. This is particularly true to analog, mixed-signal (AMS) and RF ICs. Similarly, IC modules and electronic systems also require dedicated ESD protection to address board level transient surge induced failures. These board level ESD protection solutions are often referred to as transient voltage suppressor (TVS) and typically integrated with filters to eliminate harmful electromagnetic interferers (EMI). In principle, ESD protection for IC, multiple-chip module (MCM), systems-in-package (SiP) and system board share the same mechanisms. On one hand, robust ESD protection is required, particularly for consumer electronics. On the other hand, ESD-induced parasitcs are inevitable that seriously affect IC, MCM, SiP and system performances. This tutorial provides a comprehensive review on ESD protection at all levels and discusses advanced co-design techniques for ESD/TVS/EMI designs for ICs, MCM's, SiP's and systems. Critical topics to be covered include ESD failure fundamentals and test models, ESD protection structures, AMS/RF ESD designs, TVS/EMI designs, mixed-mode ESD simulation-design methodology, ESD design optimization and prediction skills, and ESD-circuit-module-system co-design techniques, etc. Practical ESD/TVS/EMI design examples will be discussed.

Biography
Education:

- State University of New York at Buffalo, Buffalo, NY, Electrical Engineering, PhD, 1996
- The Chinese Academy of Sciences, China, Electrical Engineering, MS, 1988
- Tsinghua University, Beijing, China, Electrical Engineering, BS, 1985

Appointments:

- Professor 2007 – Present
  Director, Laboratory for Integrated Circuits and Systems, University of California, Riverside
  Director, Ubiquitous Communication by Light Center (UC-Light), University of California
  Dept. of Electrical Engineering, University of California, Riverside, CA

- Assistant/Associate Professor 1998 – 2007
  Director, Integrated Electronics Laboratory,
  Dept. of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL

- Staff R&D Engineer 1995 – 1998
  Advanced Development Group, National Semiconductor Corp., Santa Clara, CA

Research Areas:
Analog/Mixed-signal/RF ICs, Integrated Design-for-Reliability, IC CAD and modeling, Nano and emerging devices and circuits.

Editorship:

- Editor, IEEE Electron Device Letters, 2003 – Present
- Associate Editor, IEEE Transactions on Circuits & Systems I, 2003-2007, 2010 – Present.
- Guest Editor, IEEE Journal of Solid-State Circuits, 2009, 2004, 2005.
- Guest Editor-in-Chief, IEEE Trans. Electron Devices, Special Issue for RF ICs, 2004.
- Associate Editor, IEEE Transaction on Circuits and Systems II, 2003.

Recent Awards and Honors:

- Fellow, AAAS, 2011.
- The Chancellor's Award for Excellence in Undergraduate Research, U of California Riverside, 2010.
- Fellow, IEEE, 2009.
- Fulbright Specialist Roast, 2009.
- Outstanding Overseas Young Scholar Award, NSF of China, 2007.
- Chunhui Outstanding Overseas Scholar, Ministry of Education of China, 2006.
- Inaugural Sigma Xi Award for Excellence in University Research, IIT, 2003.

- National Science Foundation CAREER Award, 2002.
- IEEE Distinguished Lecturer, IEEE Electron Device Society, 2002 - Present.
- IEEE Distinguished Lecturer, IEEE Solid-State Circuit Society, 2001 - 2008.

Professional & Committee Services:
- Secretary, IEEE CAS ASPTC Committee, 2011-Present.
- Vice President, IEEE Electron Device Society, 2006–Present.
- ExCom member, IEEE EDS, 2006-Present.
- AdCom member, IEEE EDS, 2003-2009, 2011-Present.
- Committee, SIA International Technology Roadmap for Semiconductors (ITRS), 2007–Present.
- Member, IEEE EDS VLSI Technology and Circuits Committee, 2002-present
- Member, IEEE CAS Analog Signal Processing Technical Committee (ASPTC), 2006-present.
- IEEE TAB MGA Board, 2010-present
- IEEE-USA Government Relations, Research & Development Policy Committee, 2010-present
- General Chair, IEEE EDSSC 2010; TPC co-Chair, IEEE ASICON 2007; Organization co-Chair, IEEE ICSICT 2006/2008; General co-Chair, IEEE IEDST 2007; Steering Committee, RFIC 2006-2011; Executive Committee, BCTM 2011; TPC member for IEEE IEDM, CICC, RFIC, RWW, BCTM, ICSICT, ASICON, IEDST, ISCAS, IEW, IRPS, ICUWB, EDSSC, ISTC, MIEL, ICEMAC, AP-RASC, ASP-DAC, NewCAS, APC-CAS, etc.

T02. Digital Delta-Sigma Modulators for DAC and Fractional-N Frequency Synthesis Applications

Prof. Michael Peter Kennedy (University College Cork, Ireland)

Delta-Sigma Modulation (DSM) is increasingly used in digital to analog converters and frequency synthesizers. Classical analysis of DSM makes assumptions about quantisation that promote linear ways of thinking. Many of the unexpected phenomena that degrade the performance of real systems are due to underlying nonlinear effects. The use of finite state machines adds a further level of complexity. This tutorial is in two parts. Part I addresses ideal Digital Delta-Sigma Modulator (DDSM), explains what signal processing assumptions are commonly made to understand its operation, and presents an overview of applications of DDSMs. Part II focuses on the real DDSM, identifying what can go wrong and why; it concludes with state of the art solutions to problems that result from nonlinearities and finite states. The key issue addressed is spurious tones: how they arise and how to eliminate them.

Biography
Michael Peter Kennedy received the BE (Electronic) from University College Dublin (UCD) in 1984, was awarded the MS and PhD in Electrical Engineering by the University of California at Berkeley in 1987 and 1991, respectively, and the Doctorate in Engineering by the National University of Ireland in 2010. He was with UCD from 1992 until 2000, when he joined University College Cork (UCC) as Professor of Microelectronic Engineering. Dr. Kennedy has published over 300 technical articles. He received the Best Paper Award from the International Journal of Circuit Theory and Applications in 1991 and delivered the 88th Kelvin Lecture to the IEE in 1997. He was made a Fellow of the IEEE in 1998 and a member of the Royal Irish Academy in 2004. He received the IEEE Millenium Medal and the IEEE CAS Society Golden Jubilee Medal in 2000. He was awarded the inaugural Parsons Medal by the Royal Irish Academy for Excellence in Engineering Research in 2001.

T03. Smart CMOS Image Sensors for 2-D and 3-D Capture and Processing: Pixels, Circuits, Architectures, and Practical Design Guidelines

Prof. Angel Rodríguez-Vázquez (University of Seville, Spain)

CMOS imagers are complex systems whose design require quite different pieces of expertise, namely: pixels, analog signal processing, pixel readout and analog-to-digital conversion, digital signal processing, output drivers, etc. Confronting the design of new imagers require hence the concourse of multidisciplinary teams. However, because correct operation call for the close interconnection among the different parts, global knowledge is mandatory for successful design. This is particularly pertinent for the newer generations of smart imagers required for high-end applications and/or requiring ultra high image capture, on-chip image correction, scene interpretation, high dynamic range capture, etc. All these features demand architectural and circuital innovations and pose significant challenges to designers. Also, the increased interest on sensors capable of capturing 3-D scenes raise new challenges at circuit level related to the necessity to interface pixels different from those employed for 2-D capture, on the one hand, and to extract and convert to digital domain time information, on the other hand..

This tutorial addresses the design of smart CMOS imagers by following a comprehensive and complete topdown approach where each subsystem is contemplated and described as a part of a whole. Starting the formulation of the performance metrics used to specify and characterize imagers, the tutorial explains how the subsystem behavior and non-idealities impact on the global imager metrics, thereby setting the basis to specify the subsystems for given global image sensor specs. Such methodology is illustrated in the tutorial via a dedicated, MATLAB-based modeling tool which will be employed to allow the attendees gaining insight on the impact of non-ideal sub-systems behaviors. The tutorial overviews the state-of-the-art regarding: pixels; analog signal processing and read-out circuitry; data conversion circuitry, covering both amplitude data converters (required for 2-D images) and time-to-digital converters (required for 3-D imagers); driving circuits. Practical design recipes are given for all these circuits. Architectures and circuit solutions employed for high dynamic range acquisition and embedded image processing are also reviewed. A case study is included where attendees are exposed to practical considerations to be taken during the design process, including the influence of packaging, optics and camera embedding.

Biography
Ángel Rodríguez-Vázquez received a PhD degree on Physics-Electronics in 1983. He is a Full Professor of Electronics at the University of Seville and the Institute of Microelectronics of Seville/CNM-CSIC. He is also the President and the responsible for long term R&D of Innovaciones Microelectrónicas S.L. (www.anafocus.com).

Prof. Rodríguez-Vázquez has always been looking for the balance between long term research and innovative industrial developments. He started a research unit on High-Performance Analog and Mixed-Signal VLSI Circuits of the Institute of Microelectronics of Seville/CNM-CSIC. He headed this unit until 2004, for more than 15 years, in the course of which he educated three generations of PhDs who are currently working at Academia and at Industry.

During these years, he conducted pioneering R&D activities on bio-inspired microelectronics, including vision chips and neuro-fuzzy interpolators and controllers. He was also a pioneer in the application of chaotic dynamics to instrumentation and communications; and his team completed the design and prototyping of the first, world-wide, integrated circuits with controllable chaotic behaviour and the design and prototyping of the first world-wide chaos-based communication MoDem chips. His team made also significant contributions to the area of structured analog and mixed-signal design and the area of data converter design, including the elaboration of advanced teaching materials on this topic for different industrial courses and the production of two widely quoted books on the design of high-performance CMOS sigma-delta converters.

Some 30 high-performance mixed-signal chips were successfully designed by his research unit at IMSECNM/ CSIC until 2001 in the framework of different R&D programs and contracts. These include three generation of vision chips for high-speed applications, analog front-ends for XDSL MoDems, ADCs for wireless communications, ADCs for automotive sensors, chaotic signals generators, complete MoDems for power-line communications, etc. Many of these chips were state-of-the-art in their respective fields. Some of them entered in massive production. During this period of time he was also active regarding industrial training. He produced teaching materials on data converters that were employed by several companies. His courses got the Quality Label of EuroPractice.

He founded Innovaciones Microelectrónicas S.L. (AnaFocus) together with some colleagues in 2001. This company started operation after raising venture capital in January 2004. He served as the AnaFocus CEO until June 2009, a period in which the company grew from 2 employees until 50 employees and reached the threshold of maturity as a worldwide company specialized in the design and production of smart CMOS imagers and vision systems-on-chip.

Since June 2009 he has been back to conduce long term research activities in the areas of vision systems using 3D integration technologies and medical electronics.

Prof. Rodríguez-Vázquez has authored/edited: 8 books; around 40 chapters in contributed books, including original tutorials on chaotic integrated circuits, design of data converters and design of chips for vision; and some 500 articles in peer-review specialized publications. He has presented many invited plenary lectures at different international conferences and has received a number of international awards for his research work (IEEE Guillemin-Cauer best paper award; the IEEE ECCTD best paper award and the IEEE ISCAS best demo-paper award) and was elected Fellow of the IEEE for his contributions to the design of chaos-based communication chips and neuro-fuzzy chips. His research work is widely quoted (some 4,500 quotes) and he has a h-index of 35.

Prof. Rodríguez-Vázquez has served and is currently serving as Editor, Associate Editor and Guest Editor for different IEEE and non-IEEE journals; he is in the committee of many international journals and conferences; and has chaired different international IEEE and SPIE conferences. Among others he has served as: TPC chair of IEEE ESSCIRC 1992 and 2010; General Chair of IEEE NDES 1996, IEEE CNNA 1996, IEEE ECCTD 2007 and IEEE ESSDERC-ESSCIRC 2010. He is currently serving as VP-R8 of CASS and is appointed as General Chair of IEEE ICECS 2012.

T04. Smart Grids, Electric Vehicles, and Energy Storage Systems: Emerging Trends, Circuits, and Devices

Prof. Gregorio Cappuccino (University of Calabria, Italy)
Dr. Francesco A. Amoroso (University of Calabria, Italy)

Owing to their significant benefits electric vehicles (EVs) are expected to spread rapidly. The additional demand for electric power required to charge a large fleet of EVs may add a remarkable load to the distribution grid, leading to possible critical overloads. To overcome these possible problems it is mandatory to develop smart grid infrastructures and charging systems which could allow implementing innovative management strategies for the EV charging processes. These strategies can be also profitably used to manage the emerging energy storage systems, which are increasingly gaining attention nowadays at the grid-scale level, but also at the commercial and residential level.

The first part of the proposed tutorial will review the state-of-the-art of battery-based energy storage systems, both for general (industrial) and automotive applications. Technology and research issues will be illustrated, as well as standardization effort in the field.

The second part of the tutorial will focus on traditional design approaches of power battery chargers essentially targeted to implement “dumb” & “fast” charging methods. Attendees will discover how advanced, high-efficiency charging methods require novel design paradigms, at device, circuit and control levels.

The third part of the tutorial will examine these aspects more deeply. Indeed, combined grid/charger management strategies to maximize the efficiency of the power flow through the whole battery system will be analyzed. Moreover, design guidelines and management strategies will be introduced for solar systems with storage capabilities in order to maximize the amount of energy stored for a given lighting condition.

After this phase, circuits and systems required to realize a smart grid capable of implementing the advanced charging/discharging strategies for EVs and energy storage systems will be treated. In particular, attention will be paid to communication systems, smart meters and smart terminals which allow implementing the smart management strategies discussed.

Biography
Prof. Gregorio Cappuccino
Born in 1967, he received the Laurea Degree (Magna cum Laude) in Computer Science Engineering from the University of Calabria (UNICAL), Italy, in 1992 and the Ph.D. degree in Electronics from the Polytechnic of Turin (Italy), in 1998. In 1993, he joined the Electronic Components and Electromagnetism Institute of National Council of Research (IRECE-CNR, now IMM-CNR), where he was involved in the design of a Synthetic Aperture Radar Data Processor. In 1998 he joined the Department of Computer Science, Electronics and Systems (DEIS) at UNICAL as Research Assistant, working on On-chip Interconnect Modelling and High-Speed Digital devices. He is currently Associate Professor of Electronics, working with the Microelectronic and Microsystems Laboratory at UNICAL. He is teaching “Advanced (Analog) Electronics”, “Analog Electronic Design” and “Electronic Technologies”.

His research activities include mixed-signal silicon circuit and system design, high speed interconnects and systems for power management. He is currently working on new architectures for fast-response amplifiers and electronic systems for high-efficiency charging of battery for next generation of electric vehicles. In these fields he has co-authored and published over 60 refereed journal and conference publications and 5 patents.
The paper “Settling Time Optimization for Three-Stage CMOS Amplifier Topologies”, authors Pugliese, A. Amoroso, F. A. Cappuccino, G. Cocorullo, G. (IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 56 Issue: 12, Dec. 2009) listed as Top 20 for IEEE Transactions on Circuits and Systems I downloaded from January - June 2010 and as the top 52 most downloaded paper in IEEE overall, December 2009 and January 2010.
He has undertaken numerous product oriented applied research and development projects/contracts for Italian corporations in the field of power management of complex systems and sensor networks. He is currently engaged in a number of European Projects dealing with Smart Grids and Energy Storage. He is a member of the IEEE Technical Committee on Analog and Signal Processing and he serves as a regular reviewer of several international journals as Proceedings of the IEEE, IET Circuits, Devices & Systems, Information Sciences, Circuit Theory and Applications and conferences.
He served as chair of the ISCAS 09 “Amplifiers II” lecture session and “Analog Circuits & IC Technology” poster session, ICECS 2009 “Analog Techniques” and “Analog Signal Processing” lecture sessions. Moreover, he served as chair of the ISCAS 2010 “Switching Amplifiers & Feedback Techniques” lecture session and “High-Speed Circuits” poster session. Since 2006 he has been Associate Editor for “Journal of Circuits, Systems and Computers”, a World Scientific Publishing Company Journal. Dr. Cappuccino is an IEEE senior member since 2008. Dr. Cappuccino was selected as the recipient of the University of Calabria Young Researchers Award for 1999 and University of Calabria Learning Enhancement Project Award in 1999. He has received the 2011 IEEE Real World Engineering Project Award for the Project “Coping with the Emerging Energy Demand for Charging Plug-in Electric Vehicles”.
In the academic years 2008-2009 and 2009-2010 he was in charge of coordinating the project for remedial classes for freshmen of the Faculty of Engineering of University of Calabria, funded by European Commission (European Social Fund – ESF) and Calabria Regional Government (170.000 and 700.000 kEuro for first and second years, respectively). He has been invited speaker at the workshop “Home Automation: back to the future”, organized by EESTEC (Electrical Engineering STudents' European assoCiation). Title of the talk “Power Line Carrier Application to Home Automation”.

Dr. Francesco A. Amoroso
Francesco Antonio Amoroso received the B.Sc. and M. Sc in Electronics Engineering from University of Calabria in 2004 and 2006, respectively, and the Ph. D. degree in Electronics Engineering in 2011 from University Mediterranea of Reggio Calabria. Since 2011, Dr. Amoroso is Research Assistant at the Department of Electronics, Computer Science and Systems of University of Calabria.
His research interests include the design of electronic systems for Smart Grids and highperformance analog integrated electronic circuits. In these fields he has co-authored and published over 20 technical papers and 5 patents.
The paper “Settling Time Optimization for Three-Stage CMOS Amplifier Topologies”, authors Pugliese, A. Amoroso, F. A. Cappuccino, G. Cocorullo, G. (IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 56 Issue: 12, Dec. 2009) listes as Top 20 for IEEE Transactions on Circuits and Systems I downloaded from January - June 2010 and as the top 52 most downloaded paper in IEEE overall, December 2009 and January 2010.
He is currently engaged in a number of European Projects dealing with Smart Grids and Energy Storage. He serves as regular reviewer for international journals and conferences. Dr. Amoroso has been selected as the recipient of the University of Calabria Young Researchers Award for 2010. He has received the 2011 IEEE Real World Engineering Project Award for the Project “Coping with the Emerging Energy Demand for Charging Plug-in Electric Vehicles”.

T05. Design and Implementation of Multi-view 3DTV System

Prof. Yo-Sung Ho (Gwangju Institute of Science and Technology, Korea)

In recent years, various multimedia services have become available and the demand for three-dimensional television (3DTV) is growing rapidly. Since 3DTV is considered as the next generation broadcasting service that can deliver real and immersive experiences by supporting user-friendly interactions, a number of advanced threedimensional video technologies have been studied. Among them, multi-view video coding (MVC) is the key technology for various applications including free-viewpoint video (FVV), free-viewpoint television (FVT), 3DTV, immersive teleconference, and surveillance systems. In this tutorial lecture, we are going to cover the current state-ofthe-art technologies for 3DTV. After defining the basic requirements for realistic broadcasting services, we will cover various multi-modal immersive media processing technologies. We also explain a hybrid camera system for multi-view 3DTV services and discuss several challenging issues of 3D video processing, such as camera calibration, image rectification, illumination

compensation and color correction. In addition, we are going to discuss the MPEG activities for 3D video coding, including depth map estimation, prediction structure for multi-view video coding, multi-view video-plus-depth coding, and intermediate view synthesis at virtual viewpoints.

Biography

Dr. Yo-Sung Ho received the B.S. and M.S. degrees in electronic engineering from Seoul National University, Seoul, Korea, in 1981 and 1983, respectively, and the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, in 1990. He joined ETRI (Electronics and Telecommunications Research Institute), Daejon, Korea, in 1983. From 1990 to 1993, he was with North America Philips Laboratories, Briarcliff Manor, New York, where he was involved in development of the Advanced Digital High-Definition Television (AD-HDTV) system. In 1993, he rejoined the technical staff of ETRI and was involved in development of the Korean DBS Digital Television and High-Definition Television systems. Since 1995, he has been with Gwangju Institute of Science and Technology (GIST), where he is currently Professor of Information and Communications Department. Since August 2003, he has been Director of Realistic Broadcasting Research Center at GIST in Korea.

He gave several tutorial lectures at various international conferences, including the IEEE International Conference on Image Processing (ICIP) in 2009 and 2010, the IEEE International Conference on Multimedia & Expo (ICME) in 2010 and 2011, and the Pacific-Rim Conference on Multimedia (PCM) in 2006 and 2008. He has been serving as an Associate Editor of IEEE Transactions on Circuits and Systems Video Technology (T-CSVT). His research interests include Digital Image and Video Coding, Image Analysis and Image Restoration, Three-dimensional Image Modeling and Representation, Advanced Source Coding Techniques, Three-dimensional Television (3DTV) and Realistic Broadcasting Technologies.

T06. Computer Algebra and Its Applications to Circuits, Signals, and Systems

Prof. Zhiping Lin (Nanyang Technological University, Singapore)
Prof. Li Xu (Akita Prefectural University, Japan)

Computer algebra is playing an increasingly important role in many engineering problems. In particular, Grobner bases, as one of the important tools in computer algebra, have found wide applications in almost every area in circuits, signals and systems. The main reason for the success of Grobner bases is that many problems in mathematics, science and engineering can be represented by multivariate polynomials (ideals, modules, matrices etc.), and Grobner bases are well known to play a similar role in multivariate polynomials as Euclidean Division Algorithm in univariate polynomials. One of the major advantages of Grobner bases, or more general, computer algebra, is that both numerical and symbolic solutions are provided when exist.

The objectives of this tutorial are threefold. Firstly, we give an elementary lecture on Grobner bases to further bring awareness of and stimulate interest in Grobner bases among researchers and engineers in circuits, signals and systems. This part includes the basic concepts, unique properties and algorithms for Grobner bases of nD polynomial ideals, such as term ordering, the division for nD polynomials, normal forms and cofactors, (reduced) Grobner basis, S-polynomials, the elimination property etc. Information about several popular software packages for Grobner bases is also provided. Secondly, we present two practical applications of Grobner bases to the testability evaluation for analog linear circuits and to signal reconstruction from multiple unregistered sets of samples. Thirdly, we give a brief survey of applications of Grobner bases to circuits, signals and systems, ranging from the analysis and design of multidimensional control systems, wavelets and filter banks to translinear network synthesis, and biological applications. Many simple examples are illustrated throughout to help participants to understand Grobner bases easily and their applications.

Biography

Prof. Zhiping Lin

Academic Qualifications:
9/1983 – 7/1987 Ph.D. degree in information engineering, University of Cambridge, U.K.
2/1978 – 1/1982 B.Eng degree in electrical engineering, South China Institute of Technology, Canton, China

Editorial Boards:
2011 – present Editor-in-Chief of the international journal of Multidimensional Systems and Signal Processing (MSSP)
2010 – present Associate Editor of IEEE Transactions on Circuits and Systems, Part II
2005 –2010 Co-Editor of MSSP

2001 Guest Co-Editor, Special Issue on "Applications of Groebner bases to multidimensional systems and signal processing," in MSSP
2000 – 2007 Associate Editor of the international journal of Circuits, Systems, and Signal Processing
1993 – 2004 Editorial board member, MSSP

International Recognition:
2011 Plenary address at the Seventh International Workshop on Multidimensional Systems, Poitiers, France
2007-2008 Distinguished Lecturer, Circuits and Systems Society, IEEE
2007 IEEE Signal Processing Society Young Author Best Paper Award (to Qiyue Zou, my former Master student) for the paper co-authored by Q. Zou, Z. Lin and R.J. Ober, "The Cramer Rao lower bound for bilinear systems," IEEE Transactions on Signal Processing, USA, vol. 54, pp. 1666-1680, May, 2006.
2003 Outstanding Reviewer, IEEE Transactions on Circuits and Systems I
1998 Plenary address at the First International Workshop on Multidimensional Systems, Lagow, Poland

Service to IEEE Circuits and Systems Society
(a) Member of DSP Technical Committee, Circuits and Systems Society, IEEE, 2001 – present
(b) Member of Life Science Systems and Applications Technical Committee, Circuits and Systems Society, IEEE, 2005 – present
(c) Chair of Singapore Chapter of Circuits and Systems, IEEE, 2007 – 2008

Total Number of Publications:
(a) Book Chapters (3)
(b) Journal Papers – Internationally Referred (83)
(c) Conferences Papers– Internationally Referred (85)

Prof. Li Xu

Education Records:
2/1978 – 1/1982 B. Eng. degree in Automatic Control, Huazhong University of Science and Technology, Wuhan, China
4/1988 – 3/1990 M. Eng. degree in Information and Computer Science, Toyohashi University of Technology, Toyohashi, Japan
4/1990 – 3/1993 Dr. Eng. degree in System and Information Engineering, Toyohashi University of Technology, Toyohashi, Japan

Academic Appointments:
4/1993 – 3/1998 Assistant Professor, Department of Knowledge-Based Information Engineering, Toyohashi University of Technology, Toyohashi, Japan
4/1998 – 3/2000 Lecturer, Department of Information Management, School of Business Administration, Asahi University, Gifu, Japan
4/2000 – 3/2007 Associate Professor, Department of Electronics and Information Systems, Akita Prefectural University, Akita, Japan
4/2007 – Present Professor, Department of Electronics and Information Systems, Akita Prefectural University, Akita, Japan

Editorial Boards:
2000.4 – Present Associate Editor of Multidimensional Systems and Signal Processing (MSSP);
2001 Guest Editor of Special Issue of MSSP: *Applications of Gr¨obner Bases in Multidimensional Systems and signal Processing*.

Service to Society:
5/2005 – Present Member of DSP Technical Committee, Circuits and Systems Society, IEEE
1/2008 – Present Member of Sendai Section Executive Committee, IEEE

Total Number of Publications:
(1) Book and Book Chapters: 6
(2) Journal Papers: 41
(3) International Conference Papers: 60

T07. On-chip High-voltage Generator Design

Dr. Toru Tanzawa (Micron Japan, Ltd., Japan)

According as silicon technology has been advanced, multiple high-voltage generation on chip is becoming one of big challenges on circuit and system design for Flash memories, LCD drivers, and other semiconductor devices to optimize entire circuit area and power efficiency with a low voltage supply. This tutorial covers all the component circuit blocks, including charge pumps, pump regulators, level shifters, oscillators, and references, in addition to an introduction to its application and entire system design. The charge pump inputs the supply voltage and a clock generated by the oscillator, and outputs a voltage higher than the supply voltage or a negative voltage. The regulator enables the charge pump when the absolute value of the output voltage of the charge pump is lower than the target voltage on a basis of a reference voltage, or disables it otherwise. The generated high- or negative-voltage is transferred to a load through high- or low-level shifters. It reviews the various charge pump topologies, including Cockcroft-Walton, parallel capacitor ladder, Dickson, Fibonacci, and 2^N. Then, the optimum topology for on-chip high-voltage generator is identified to be Dickson's liner charge pump taking parasitic capacitance into consideration. Various equivalent circuit models for the linear pump are described to minimize the circuit area to meet the constraint on the output current and the rise time and to minimize the power to meet the constraint on the output current. Level shifters are also reviewed such as CMOS high level shifter, NMOS high level shifter, high voltage depletion NMOS + PMOS level shifter, and CMOS low level shifter. The tutorial then shows some practical examples of charge pump circuits such as threshold voltage compensation, structure reconfiguration, and noise reduction techniques. It also introduces design methodology for multiple high-voltage generator system and modelling for effective full-chip verification.

Biography
Toru Tanzawa is Principal Design Engineer at Micron Technology in Tokyo, Japan. He is currently involved in the design of analogue circuits for multi-level cell NAND Flash memories. In the past he also worked for Toshiba as Design Engineer for high-density NAND and high-speed low-voltage NOR Flash memories as well as for RF-CMOS wireless LSI's for Bluetooth. He received the B.S. degree in physics from Saitama University, Japan, in 1990, the M.S. degree in physics from Tohoku University, Japan, in 1992, and the Ph.D. degree in electrical engineering from the University of Tokyo, Japan, in 2002, respectively. He holds over 110 U.S. patents and has published over 30 papers in IEEE conferences and journals. Toru Tanzawa is a senior member of IEEE.

T08. High-/Mixed-Voltage Analog and RF Circuits and Systems for Wireless Applications

Prof. Elvis, Pui-In Mak (University of Macau, China)
Prof. Rui Paulo da Silva Martins (University of Macau, China)

IC designers may have already experienced the shortcomings of low supply voltage (VDD) in ultra-scaled CMOS technologies. High-VDD and mixed-VDD techniques are emerged as a potential solution to deal with the problems induced by low-voltage constraints. By exploiting the well-established features of nanoscale processes such as: MOSFETs with multiple oxide thicknesses and VDD driving capability, the performances of analog and RF circuits can be cost-efficiently improved. For instance, a hybrid use of core and I/O VDD's, thin-oxide and thick-oxide MOSFETs directly open up much freedom in topology selection, while fully benefiting the speed and area improvements of advanced processes. The key concern is on the circuit reliability which, however, can be ensured via proper biasing and use of startup/protection circuitry; both induce neglectable cost.
This tutorial aims to provide an overview of the basic principles, system design considerations and examples relevant to high-VDD and mixed-VDD analog and RF circuits design. A wide variety of topologies from the literature are examined and new topologies are proposed; all achieved state-of-the-art performances in silicon. Novel voltage-conscious circuit concepts generally extendable to other wireless systems are discussed, aiming to demonstrate how analog and RF circuits can be improved effectively in ultra-scaled CMOS technologies using purely circuit-level techniques.

Biography

Prof. Elvis, Pui-In Mak

Research Statistics:
2 Scientific books (Springer Press)
20 Scientific journal papers (mostly with IEEE and IET)
59 Scientific conference papers
10 Invited international presentations
3 US patents

Professional Journal Editorship:
2010-2011 IEEE Transactions on Circuits and Systems I – Regular Papers
2010-2011 IEEE Transactions on Circuits and Systems II – Express Briefs

Professional Society Leadership:
2009-2011 Board of Governors, IEEE Circuits and Systems Society

State-Key Lab Research Leadership:
2008-Present Coordinator of Wireless and Biomedical Research Lines, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau

Conference Organization and Referees of Scientific Publications:
2003-Present Steering/Organization Committee Member of 7 Conferences
2003-Present Technical Program Committee Member/Chair of 16 Conferences
2003-Present Referee of 3 Books, 18 Journals and 9 conferences

Granted US Patents:
1. Pui-In Mak, Seng-Pan U, R. P. Martins, Two-Step Channel Selection for Wireless Transmitter Front-Ends, US Patent, Granted, No. 2008/0318534.
2. Pui-In Mak, Seng-Pan U, R. P. Martins, DC-Offset Canceled Programmable Gain Array for Low-Voltage Wireless LAN System and Method Using the Same, US Patent, Granted, No. 7,948,309.
3. Pui-In Mak, Seng-Pan U, R. P. Martins, Two-Step Channel Selection for Wireless Receiver Front-Ends, US Patent, Granted, No. 7,529,322

Prof. Rui Paulo da Silva Martins

Rui Paulo da Silva Martins (IEEE Member'88 – Senior Member'99 – Fellow'08), born in April 30, 1957, received the Bachelor (5-years), the Masters, and the Ph.D. degrees as well as the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992 and 2001, respectively. He has been with the Department of Electrical and Computer Engineering / IST, TU of Lisbon, since October 1980.

Since 1992, he has been on leave from IST, TU of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is a Full-Professor since 1998. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment as Vice-Rector (Research) until August 31, 2013. Within the scope of his teaching and research activities he has taught 20 bachelor and master courses and has supervised 24 theses, Ph.D. (11) and Masters (13). He has published: 16 books, co-authoring (5) and co-editing (11), plus 5 book chapters; 204 refereed papers, in scientific journals (38) and in conference proceedings (166); as well as other 70 academic works, in a total of 295 publications. He has co-authored 3 US Patents (1 issued in 2009 and 2 in 2011) and has also submitted other 4. He has created the Analog and Mixed-Signal VLSI Research Laboratory of UM: http://www.fst.umac.mo/en/lab/ans_vlsi/website/index.html, recently elevated to State Key Lab of China (the 1st in Engineering in Macao), being its Founding Director.

Prof. Rui Martins is an IEEE Fellow, was the Founding Chairman of IEEE Macau Section from 2003 to 2005, and of IEEE Macau Joint-Chapter on Circuits And Systems (CAS) / Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of the IEEE Circuits And Systems Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits And Systems – APCCAS'2008, and was elected Vice-President for the Region 10 (Asia, Australia, the Pacific) of IEEE CASS, for the period of 2009 to 2012. He is Associate Editor of the IEEE Transactions on Circuits and Systems II: Express Briefs, for the period of 2010 to 2011. He was the recipient of 2 government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999,

and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences, Lisbon, Portugal.

T09. Advances in Speech Coding, Speech Recognition, and Applications

Prof. Tokunbo Ogunfunmi (Santa Clara University, USA)
Dr. Madihally (Sim) Narasimha (Qualcomm, Inc., USA)
Prof. Roberto Togneri (The University of Western Australia, Australia)

Speech Coding1 refers to the digital representation of the information-bearing analog speech signal, with emphasis on removing the inherent redundancies. Efficient coding of speech waveforms is essential in a myriad of transmission and storage applications such as traditional telephony, wireless communications (e.g., mobile phones), internet telephony, voice-over-internet protocol (VoIP), and voice mail. Many of these applications are currently going through an impressive growth phase.
Speech Recognition encompasses a range of diverse technologies from engineering, signal processing, mathematical statistical modeling and computer science language processing necessary to achieve the goal of human-computer interaction using our most natural form of communication: speech. Applications of speech recognition have exploded due to the advent of smartphone technology where the use of the traditional keyboard and mouse has given way to touch and speech, and in enterprise automated computer voice response services for enquiries and transactions. We are now experiencing an exponential growth in the adoption of speech recognition in smartphone and mobile technology, in information and transaction services and increased R&D effort on efficient low-cost and low-power implementations, robustness in the presence of ambient noise and reliable language understanding and dialog management.
The aim of this tutorial is to introduce the basic principles underlying the generation, coding and transmission of speech. First, we present the two major speech coding schemes-- waveform coding and parametric coding—and delineate the fundamental principles behind the coding methods used therein. Then, we discuss examples of speech coding standards in use today and the practical implementation of a popular standardized speech coder e.g. on a DSP processor.
We also present practical speech coding methods and signal processing algorithms to combat impairments in VoIP systems. We use the recently developed and popular internet low bit-rate coder (iLBC) as an example of necessary modifications to existing speech coders to enhance performance, when deployed in a new medium. We present recent research results in the field of speech coding related to this.
We discuss the recent standardization efforts and the future challenges in the field of speech coding. These challenges will serve as catalyst for ISCAS attendees to spur new contributions to this exciting and constantly growing field.
We also present basic processing and modeling paradigms required for successful speech recognition systems. First, we discuss the important issue of how relevant time-frequency features are extracted from the speech signal in a form suitable for statistical modeling. Second, we present the Hidden Markov Model (HMM) as the key technology which has been developed to handle the complex task of modeling speech and recognizing words. Finally, we highlight the importance of language modeling in using knowledge of the language structure to refine and streamline the HMM recognition process and produce grammatically correct transcriptions of English speech. We will present the discussion of the theory and algorithms in the context of using the popular research HMM software toolkit, HTK, to implement a basic speech recognition system.
We hope the material presented here will educate new comers to the field and also help elucidate to practicing engineers (involved in both algorithm and implementation issues) and researchers the important principles of speech coding with applications in many devices and applications such as wireless communications (e.g. mobile phones), voice-over-IP, internet telephony, video comm., speech recognition, text-to-speech, etc. which are ubiquitous today.

Biography

Prof. Tokunbo Ogunfunmi
Dr. Tokunbo Ogunfunmi (Senior Member, IEEE) is currently the Associate Dean for Research and Faculty Development in the School of Engineering at Santa Clara University (SCU), Santa Clara, CA. He is also an Associate Professor in the department of Electrical Engineering and Director of the Signal Processing Research Lab. (SPRL). Previously, in 2003, he served for six months as Acting Chair of the Dept. of Electrical Engineering.
His research interests include Digital Signal Processing, Adaptive and nonlinear filters, Multimedia (Video/Audio/Speech), neural networks and VLSI/FPGA/DSP development. He has published two books and 140+ papers in refereed journal and conference papers in these and related areas.
He is a Senior Member of the Institution of Electrical and Electronic Engineers (IEEE), a Member of Sigma Xi (the

Scientific Research Society), and a Member of the American Association for the Advancement of Science (AAAS). He is a member of the IEEE CASS Technical Committees (TC) on Digital Signal Processing (DSP) and Circuits and Systems for Communications (CASCOM). He serves as the Secretary of the CASS Technical Committee on Circuits and Systems for Education Outreach (CASEO). Previously, he served as Chair of the IEEE Signal Processing Society (SPS) Santa Clara Valley Chapter (2007-2009) and is a member of the SPS TC on DISPS.
He is an Associate Editor of the journal Circuits, Systems and Signal Processing. He has served on many IEEE Conference Committees as Member of the Organizing and Technical Committees. He also served as Technical Program Chair of the 2nd IEEE Conference on Adaptive Science and Technology, Dec. 2009 and gave a keynote talk.
Dr. Ogunfunmi has been a consultant to industry and government, and a visiting professor at The University of Texas and Stanford University. His industrial experience includes consulting for companies such as Broadcom, AMD, CASE Technology, CLARIS Corp., Clairvoyant, NEC, AT&T Bell Labs. and NIKON Precision Research & Development. He is also a registered professional engineer. He obtained his PhD in Electrical Engineering from Stanford University.

Dr. Madihally (Sim) Narasimha

Madihally (Sim) Narasimha has more than twenty years of experience in the telecommunications and networking industries. He is currently a Senior Director of Technology at Qualcomm Inc., Santa Clara, CA. Prior to joining Qualcomm, he was Vice President of Technology at Ample Communications, where he directed the development of Ethernet physical layer chips. Prior to that, he served in technology leadership roles at several Voice-over-IP (VoIP) startup companies including IP Unity, Realchip Communications, and Empowertel Networks. He also held senior management positions at Symmetricom and Granger Associates, where he was instrumental in bringing many DSP-based telecommunications products to the market.
His research interests include digital signal processing algorithms for wireless and baseband communication receivers, signal processing techniques to improve speech quality in Voice-Over-IP (VoIP) systems, and voice/video compression algorithms. He has authored one book, five patents, and over forty refereed journal and conference papers in these and related areas. He has also served as a guest editor for two special issues of the IEEE transactions on applications of digital signal processing.
Currently he also serves as a Consulting Professor of Electrical Engineering at Stanford University, Stanford, CA, where he developed a new academic program in the telecommunications area by introducing two new courses: Digital Transmission Systems in Telecommunications and Digital Switching Systems in Telecommunications into the Stanford curriculum. He is also a Lecturer in Electrical Engineering at Santa Clara University, Santa Clara, CA, where he teaches speech coding and wireless communications courses.
Dr. Narasimha obtained his M.S. (EE) and Ph.D. (EE) degrees from Stanford University, Stanford, CA. He is a Fellow of the Institution of Electrical and Electronic Engineers (IEEE).

Prof. Roberto Togneri

Dr Roberto Togneri is currently an Associate Professor with the School of Electrical, Electronic and Computer Engineering at the University of Western Australia. He was the Deputy Head of School from 2007 to 2008 and currently serves on the Engineering and Mathematical Sciences Faculty committee overseeing the implementation of the engineering foundation units for the New Courses Curriculum from 2012. Dr Togneri was also the recipient of a Faculty excellence in teaching award in 2008 and has had 5 nominations for teaching excellence.
His research activities include signal processing and robust feature extraction of speech signals, statistical and neural network models for speech and speaker recognition, audio-visual recognition and biometrics, and related aspects of communications, information retrieval, and pattern recognition. He has published 90 over papers in book chapters, refereed journals and international conferences in the areas of spoken language and information systems. He was co-author of the books “Fundamentals of Information Theory and Coding Design”, Chapman & Hall/CRC, 2003 and “Auditory Features for Speech Recognition and Enhancement”, VDM Verlag, 2009, is the chief investigator on two Australian Research Council Discovery Project research grants from 2010 to 2013, and is the lead local organizer of the AusTalk: Audio-Visual Corpus of Australian Speech initiative.
Dr Togneri also served on the Technical Program Committee of the International Speech Communication Association (ISCA) InterSpeech 2008, and the Asian Pacific Communications Conference (APCC) 2005, and is currently on the editorial board of the International Journal of Emerging Sciences (IJES). He is a member on the executive of the Australasian Speech Science and Technology Association (ASSTA), senior member of the IEEE and a member of the International Speech Communication Association (ISCA).

T10. Small Scale Energy Harvesting (EH) – Principles, Practices, and Future Trends

Prof. Dong S. Ha (Virginia Tech, USA)

Harvesting small scale energy from otherwise wasted ambient energy sources has attracted immense research efforts for applications such as battery-powered wireless sensor networks for structural monitoring, industrial condition monitoring and healthcare. The power level for those applications ranges from microwatts to milliwatts. Energy scavenged from ambient sources may be able to recharge or even replace the battery to power up those devices perpetually. Sources of energy for harvesting include, but are not limited to, light, thermal gradient, vibration, air flow, and radio frequency radiation. The fluctuation and intermittence of these ambient energy sources pose severe technical challenges to develop practical self-powered systems. Further, energy storage devices like rechargeable battery or supercapacitor as well as efficient power management circuitry are indispensable to convert a dynamic environmental energy input into a stable power source. This tutorial reviews principles of energy harvesting, practices for small scale energy harvesters, and self-powered wireless sensor modules developed recently in industry and academia. The industry trends and possible research issues for further developments are also discussed to provide a technical insight into energy harvesting techniques and their applications.

Biography

Education:
Ph.D., Electrical and Computer Engineering, University of Iowa, 1986
M.S., Electrical and Computer Engineering, University of Iowa, 1984
B.S., Electrical Engineering, Seoul National University, 1974

Teaching Interests:
Analog and Mixed-signal IC design, RF IC Design, VLSI Design, Low-power VLSI Design

Recognition:
IEEE Fellow for leadership in VLSI design and test

T11. Challenges and Opportunities in Internet of Things

Dr. Yen-Kuang Chen (Intel Labs, USA)
Prof. Chih-Ting Lin (National Taiwan University, Taiwan)

Digital sensing, processing, and communication capabilities will be ubiquitously embedded into everyday objects, turning them into an Internet of things (IoT, also known as, machine-to-machine, M2M). More importantly, everyday objects will become data generators, with sensors everywhere continuously collecting a large quantity of data about their context and use, processors everywhere analyzing and inferring useful knowledge from the data, and finally communication radios transmitting and exchanging useful knowledge with other everyday objects and to —cloud based resources. These technologies enable the new conception that our physical environment is one gigantic information creation, collection, transmission, and analysis system. This is the next-generation Internet – rather than data mainly produced by humans and for humans, in the new machine-to-machine-era Internet, data are generated by machines (sensors), communicated without human involvement to other machines (servers or other computer systems) for automated processing to enable automated or human actions, driving speeds and scales unseen by the existing Internet.
To follow the emerging IoT demands, the design paradigm of circuit and system is needed to be reconsidered. The demands result from the intelligent and secure interaction and information sharing among connected devices in IoT. These bring up numerous challenges and opportunities to engineering. In specific, the multiple disciplinary knowledge, including electronics, physics, and chemistry are needed to be fused to achieve IoT technologies. In addition, different technological thrusts, such as low-power device, reliable wired/wireless communication, mobile devices, reconfigurable network platform, autonomous deployment, robust system, and heterogeneous system are necessary to be seamless integrated. To bring up these issues and challenges, in this tutorial, we will provide a survey of the emerging IoT applications, an overview of challenges/opportunities in IoT, and examples of specific fields such as distributed video coding and energy-efficient sensors.

Biography

Dr. Yen-Kuang Chen

▶ Ph.D. from Princeton University
▶ Principal Research Scientist at Intel Labs
▶ Research interests: developing innovative technologies to address core challenges in connected context computing, including sensing, communication, context analysis, and smart services.

▶ Editorial board member
o IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2010-present.
o IEEE Signal Processing Magazine, 2010-present.
o Journal of Signal Processing Systems, 1999-present.

▶ Associate editors
o IEEE Transactions on Multimedia, 2009-present.
o IEEE Transactions on Circuit and System for Video Technology, 2008-present.
o IEEE Transactions on Circuit and System I, 2004-2005.

▶ Technical committee member
o Multimedia Signal Processing, IEEE Signal Processing Society, 2008-present.
o Multimedia Systems and Applications, IEEE Circuits and Systems Society, 2008-present.
o Visual Signal Processing and Communications, IEEE Circuits and Systems Society, 2008-present.
o Design and Implementation of Signal Processing Systems, IEEE Signal Processing Society, 2009-present.

▶ Program committee member of 35+ international conferences on multimedia, video compression/communication, image/signal processing, VLSI circuits and systems, parallel processing, and software optimization.
▶ 20 granted patents, 25 pending patent applications, and 85+ publications.
▶ Tutorial speakers at ICME 2010, ISCAS 2009, ICASSP 2009, ICASSP 2008, ICME 2007, ICASSP 2007.

Prof. Chih-Ting Lin

▶ Ph.D. from University of Michigan – Ann Arbor
▶ Assistant professor at Department of Electrical Engineering, National Taiwan University
▶ Research interests: wireless sensor network technology, sensor technologies, biochips, bio-molecular detection devices, inkjet printing fabrication process.

▶ Editorial board member,
o International Journal of Automation and Smart Technology, 2010-present.

▶ 2 granted patents, and 57 publications in journals or conferences
o Lin, C.-T., Hsu, C.-H., Chen, Y.-J., Lee C.-H., and Wu, W.-J., “Enhancement of Carrier Mobility in All-Inkjet-Printed Organic Thin-film Transistors Using a Blend of Poly(3-hexylthiophene) and Carbon Nanoparticles,” Thin Solid Films, 2011 pp. 8008-8012 DOI: 10.1016/j.tsf.2011.05.071.

o Huang, J.-D., Lee, C.-K., Yeh, C.-S., Wu, W.-J., and Lin, C.-T., “High Precision Ultrasonic Ranging System Using a Self-Interference Technique,” IEEE Transaction of Instrumentation and Measurement, 2011 (in press).

o H. R. Lin, C. S. Chen, P. Y. Chen, F. J. Tsai, J. D. Huang, J. F. Li, C.-T. Lin, and W.J. Wu, “Design of Wireless Sensor Network and Its Application for Structure Health Monitoring of Cable-stayed Bridge,” Smart Structures and Systems, 6, pp. 939-951, 2010.

o Lin, C.-T. and Huang, C.-W., “Low-Power and High-Sensitivity Humidity Sensor Using Fe-Al-Polyaniline Blends,” IEEE Sensors Journal, 10, 6, pp1142-1146, 2010.

o J.-Y. Han, H.-P. Tserng, C.-T. Lin, “Quality Assessment for Lidar Point Cloud Registration Using In-Situ Conjugate Features,” IEEE International Geoscience and Remote Sensing Symposium, Vancouver, Canada, July, 2011.

o J.-D. Huang, W.-J. Wu, J.-Y. Han, H.-P. Tserng, and C.-T. Lin, “High efficient synchronization on demand protocol of IEEE 802.15.4 wireless sensor network for construction monitoring,” The 28th International Symposium on Automation and Robotics in Construction, Seoul Korea, June 2011.

o S.-K. Hsu, H.-P. Yueh, C.-T. Lin, and Y.-J. Liu, “Exploring concept learning in a wireless sensor networking environment: A Chinese language example,” International Conference on Cognition and Exploratory Learning in Digital Age (CELDA 2010), Timisoara, Romania, Oct. 2010

T12. Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyberphysical System Integration

Prof. Krishnendu Chakrabarty (Duke University, USA)
Prof. Tsung-Yi Ho (National Cheng Kung University, Taiwan)

This tutorial is a revised and substantially updated version of the tutorial presented at ISCAS 2008 and ISCAS 2009. The earlier half-day tutorial offerings were focused on first-generation biochips, and covered the basic principles of microfluidics, chip design, and design automation. The feedback from the attendees was that a full-day tutorial was more appropriate and the content related to physics was less interesting than the design-related material.
This tutorial proposal incorporates the above feedback and it also includes recent advances in this field. In addition to fundamental concepts, it includes a more detailed presentation on application-driven chips, namely chips for immunoassays and protein crystallization. The presenters will include material on technological advances in recent years at several universities. In past years, the field was very new and most of the research results had been reported from Duke University. In recent years, there have many advances reported from other universities and research labs in the US, Taiwan, Korea, Denmark, France, etc., and attendees will learn about these new developments. In particular, sensing technology has made great strides in recent years, therefore the presenters will describe several new types of on□chip sensors for biochips. In addition, they will describe how these sensors allow on-chip error recovery through concepts such as checkpointing and rollback recovery that are common in commuting systems today. Dynamic adaptation through cyberphysical system integration will be included in the tutorial. Prof. Ho will join Prof. Chakrabarty to strengthen the design automation and the chip/fluidics co-design aspects of the tutorial offering.
The tutorial offers attendees an opportunity to bridge the semiconductor ICs/system industry with the biomedical and pharmaceutical industries. The tutorial will first describe emerging applications in biology and biochemistry that can benefit from advances in electronic “biochips”. The presenter will next describe technology platforms for accomplishing “biochemistry on a chip”, and introduce the audience to micoarrays and fluidic actuation methods based on microfluidics. The droplet-based "digital" microfluidic platform based on electrowetting will be described in considerable detail. Next, the presenter will describe fabrication techniques for digital microfluidic biochips, followed by computer-aided design, design-for-testability, cyberphysical integration, and reconfiguration aspects of chip/system design. Synthesis algorithms and methods will be presented to map behavioral descriptions to a digital microfluidic platform, and generate an optimized schedule of bioassay operations, chip layout, and droplet-flow paths. In this way, the audience will see how a “biochip compiler” can translate protocol descriptions provided by an end user (e.g., a chemist or a nurse at a doctor’s clinic) to a set of optimized and executable fluidic instructions that will run on the underlying digital microfluidic platform.
Testing techniques will be described to detect faults after manufacture and during field operation. A classification of defects will be presented based on data for fabricated chips. Appropriately fault models will be developed and presented to the audience. Online and offline reconfiguration techniques will be presented to bypass faults once they are detected. The problem of mapping a small number of chip pins to a large number of array electrodes will also be covered. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial.

Biography

Prof. Krishnendu Chakrabarty
Krishnendu Chakrabarty received the B. Tech. degree from the Indian Institute of Technology, Kharagpur, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively. He is now Professor of Electrical and Computer Engineering at Duke University. He is also a Chair Professor in Software Theory at Tsinghua University, Beijing, China. Prof. Chakrabarty is a recipient of the National Science Foundation Early Faculty (CAREER) award, the Office of Naval Research Young Investigator award, the Humboldt Research Fellowship from the Alexander von Humboldt Foundation, Germany, and several best papers awards at IEEE conferences.
Prof. Chakrabarty’s current research projects include: testing and design-for-testability of integrated circuits; digital

microfluidics, biochips, and cyberphysical systems; optimization of digital print and production system infrastructure. He has authored 10 books on these topics (with two more books in press), published over 380 papers in journals and refereed conference proceedings, and given over 170 invited, keynote, and plenary talks. Prof. Chakrabarty is a Fellow of IEEE, a Golden Core Member of the IEEE Computer Society, and a Distinguished Engineer of ACM. He was a 2009 Invitational Fellow of the Japan Society for the Promotion of Science (JSPS). He is a recipient of the 2008 Duke University Graduate School Dean's Award for excellence in mentoring, and the 2010 Capers and Marion McDonald Award for Excellence in Mentoring and Advising, Pratt School of Engineering, Duke University. He served as a Distinguished Visitor of the IEEE Computer Society during 2005-2007, and as a Distinguished Lecturer of the IEEE Circuits and Systems Society during 2006-2007. Currently he serves as an ACM Distinguished Speaker, as well as a Distinguished Visitor of the IEEE Computer Society for 2010□2012. He has presented full-day and half□day tutorials at numerous conferences, e.g., ICCAD 2010 (with Prof. Tsung-Yi Ho), ESWeek 2011 (with Prof. Tsung-Yi Ho), ISCAS 2008-2009, ASPCCAS 2010, DATE 2007, ITC 2010-2011, and DAC 2011.
Prof. Chakrabarty is the Editor-in-Chief of IEEE Design & Test of Computers and ACM Journal on Emerging Technologies in Computing Systems. He is also an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Circuits and Systems II, and IEEE Transactions on Biomedical Circuits and Systems. He serves as an Editor of the Journal of Electronic Testing: Theory and Applications (JETTA).

Prof. Tsung-Yi Ho
Tsung-Yi Ho received his Ph.D. degrees in Electrical Engineering from National Taiwan University, Taipei, Taiwan, ROC, in 2005. He is now an Assistant Professor with the Department of Computer Science and Information Engineering, National Cheng Kung University, Tainan, Taiwan, ROC. From 2003 to 2004, 2005, and 2008, he was a visiting scholar at University of California, Santa Barbara in USA, Waseda University in Japan, Synopsys in USA, respectively. His current research interests include physical design automation for nanometer ICs and digital microfluidic biochips. Since 2008 he is the principal investigator of the National SoC project in Taiwan focusing on CAD for biochips. He was a 2011 Invitational Fellow of the Japan Society for the Promotion of Science (JSPS). He has been working very closely with the semiconductor industry such as Himax, Synopsys and TSMC on projects and has co□authored a book on routing (Springer, 2007) and published papers at premier conferences/journals such as DAC, ICCAD, ISPD, ICCD, and TCAD. He has presented tutorials and organized special sessions on CAD for digital microfluidic biochips at numerous conferences, e.g., ICCAD 2010, MWSCAS 2011, SOCC2011, ESWeek 2011.

T13. Design-Oriented Analysis and the Pedagogy of Digital and Analog Filters

Prof. Babak Ayazifar (University of California Berkeley, USA)
Prof. Bharathwaj Muthuswamy (Milwaukee School of Engineering, USA)

In this education-focused tutorial, we demonstrate a way to teach EECS undergraduates to conceive, analyze, design, and implement a broad range of digital and analog filters for a variety of applications. Starting with simple, yet pedagogically rich examples, we scaffold toward more sophisticated filters with even richer behaviors. In many cases, we discuss the interrelation between the time-domain and frequency-domain features of these systems.
Filters whose design and applications we can teach undergraduate students include lowpass, highpass, bandpass, comb, notch, anti-notch, and allpass filters. We emphasize the value of back-of-the-envelope analysis and design, especially one that exploits geometric or algebraic structure to produce what the late R. D. Middlebrook of Caltech dubbed "low-entropy" ex-pressions and plots. Through software simulation or hardware implementation in a laboratory environment, students confirm their theoretical analyses. This approach not only cultivates robust analytical and design skills, but also instills deeper insight in our students. By way of example, we show how to design a filter that suppresses a 60 Hz power-line hum in an electrocardiogram (ECG) signal. Using simple geometric reasoning on, and inside, the unit circle, we design a second-order digital notch filter. Then we ask whether an analog counterpart could achieve similar results. As it turns out, passive analog circuits are unsuitable for this purpose. Therefore, we explore the design of an operational-amplifier gyrator that inverts a capacitor impedance to emulate the impractical inductor (on the order of 10 Henrys) that the passive-circuit implementation demands. An important aspect of our tutorial is that it demonstrates how we can expose students to sophisticated skills and interesting applications well before the full-scale machinery of the Fourier, Laplace, or Z transforms. In fact, we assume little more than a rudimentary knowledge of LTI systems, including the notions of impulse response and frequency response.

Biography

Prof. Babak Ayazifar
Babak Ayazifar earned his B.S. degree in EE from Caltech, and his S.M. and Ph.D. degrees in EECS from MIT. He joined the EECS faculty at UC Berkeley in 2005, where he is now a Lecturer with Security of Employment (Lecturer SOE)—equivalent to an Associate Professor in Teaching with tenure.

At MIT, Babak received the Harold L. Hazen Award for outstanding teaching. He advanced to the rank of Instructor-G, which conferred teaching assignments ordinarily reserved for faculty. And he won the Goodwin Medal, MIT's prestigious award for a graduate student whose teaching is "conspicuously effective over and above ordinary excellence." In spring 2002, he took leave from his graduate studies to assume an appointment as a Senior Lecturer in the School of Engineering, teaching a graduate course in digital signal processing. At UC Berkeley, the focus of his activities has been pedagogy—teaching, learning, curriculum development and reform, and mentoring graduate and undergraduate teaching assistants. In spring 2008, Babak received the EE Division's Outstanding Teaching Award for Excellence in Teaching.

Prior to his doctoral studies, Babak was with David Sarnoff Research Center, where he worked on digital video applications in direct-broadcast satellite and high-definition television. In his doctoral research at MIT, he used spectral graph theory to explore the mutual influence of a network's topology and dynamics; this led to his dissertation, Graph Spectra and Modal Dynamics of Oscillatory Networks.

After his doctorate, Babak joined the Intellectual Property and Technology Group of the corporate law firm Ropes & Gray, LLP, as a Technical Specialist engaged in patent prosecution and related activities. His intellectual property experience spans a wide range of technologies, including mechanical devices, intravascular MRI, DNA Microarray data analysis, and encrypted communication using chaotic systems. Babak is a patent agent, registered to practice before the United States Patent and Trademark Office (Reg. No. 56793).

Prof. Bharathwaj Muthuswamy

Affiliations:
Milwaukee School of Engineering; Department of EECS
University of California, Berkeley; Department of EECS

Research Areas:
Nonlinear Dynamical Systems, Embedded Systems, Education

Education:
Ph.D. in Electrical Engineering,
December 2009, University of California, Berkeley
Thesis: Contributions to the Study of Autonomous Chaotic Circuits and Cellular Automata
Concentration: Nonlinear Dynamical Systems
Dissertation Committee: Dr. Leon Chua (advisor), Dr. Pravin Varaiya and Dr. Andrew Szeri

M.S. in Electrical Engineering,
May 2005, University of California, Berkeley
Thesis: Implementing Central Pattern Generators for Bipedal Walkers Using CNN
Concentration: Robotics, Neural Networks and Nonlinear control/circuits
Advisor: Dr. Leon Chua

B.S. in Electrical Engineering (Honors),
August 2002, University of California, Berkeley
Concentration: Circuits and Systems

Awards:
2010 Faculty Endowment Award, Milwaukee School of Engineering
2009 New Kind of Science Summer School Fellow, CNR-Istituto ISTI, Pisa, Italy
Lecturer Teaching Fellow, 2008 – 2009, University of California, Berkeley
EECS Department GSR Fellowship, Spring 2008, University of California, Berkeley
Research Mentor Award, Summer 2007, University of California, Berkeley LEADS
Outstanding GSI Award, 2006 – 2007, University of California, Berkeley

Research and Education:
Assistant Professor of Electrical Engineering
September 2009 - Present
Milwaukee School of Engineering, Milwaukee, WI
http://myweb.msoe.edu/~muthuswamy

- o Investigate mathematical properties, circuit realizations and applications of memristors
- o Investigate relationship between dynamic systems, number theory and knot theory
- o Design embedded systems (FPGA) courses for junior undergraduate students
- o Design nonlinear dynamics course for junior undergraduates
- o Prepare lecture notes and teach courses in control theory, digital logic and basic electronics
- o Investigate alternate FPGA platforms for use in EE3921 (Digital Systems Design)

Visiting Lecturer and Graduate Student Instructor
September 1999 – September 2008
University of California, Berkeley

- o Prepared lecture notes for classes of approximately 100 students in topics on basic linear and nonlinear circuit analysis, control theory and systems theory
- o Assisted students in applying circuit analysis techniques to understand linear (resistive, capacitive and amplifier) circuits and nonlinear (diodes, oscillator) circuits
- o Coordinated teaching assistants and readers to ensure smooth operation of courses
- o Developed exercises using MATLAB and Simulink to illustrate concepts covered in lecture
- o Redesigned various laboratory experiments in different courses to coordinate closely with lecture material